The Dirty-Block Index

Vivek Seshadri*, Abhishek Bhowmick*, Onur Mutlu*, Phillip B. Gibbons†, Michael A. Kozuch†, Todd C. Mowry* (*CMU, †Intel)

Agressive DRAM-aware Writeback
1. Writes are buffered and served together
2. Row hits faster/more efficient=row misses
Writeback dirty blocks of same DRAM row together!

Problem with current organization: Several tag store lookups required

Evicted Dirty Block

Look up only dirty blocks of the same row and write them back

Cache Lookup Bypass
Bypass the lookup for an access that is likely to miss in the cache!

Problem with current organization: Cannot bypass lookup for dirty block

Reducing ECC Overhead
Store ECC only for dirty blocks. Store only EDC for clean blocks!

Problem with current organization: Any cache block can be dirty

8% Reduction in Cache Area

Load balancing accesses to cache and memory · Cache flushing (power down banks, persistent memory)
Efficient bulk DMA · Efficient memory write scheduling · Reducing metadata overhead for dirty blocks

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