The Efficacy of Error Mitigation Techniques for DRAM Retention Failures

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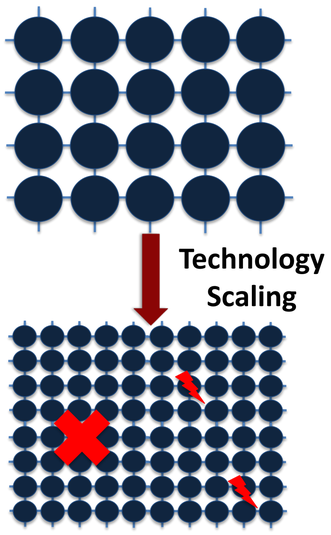
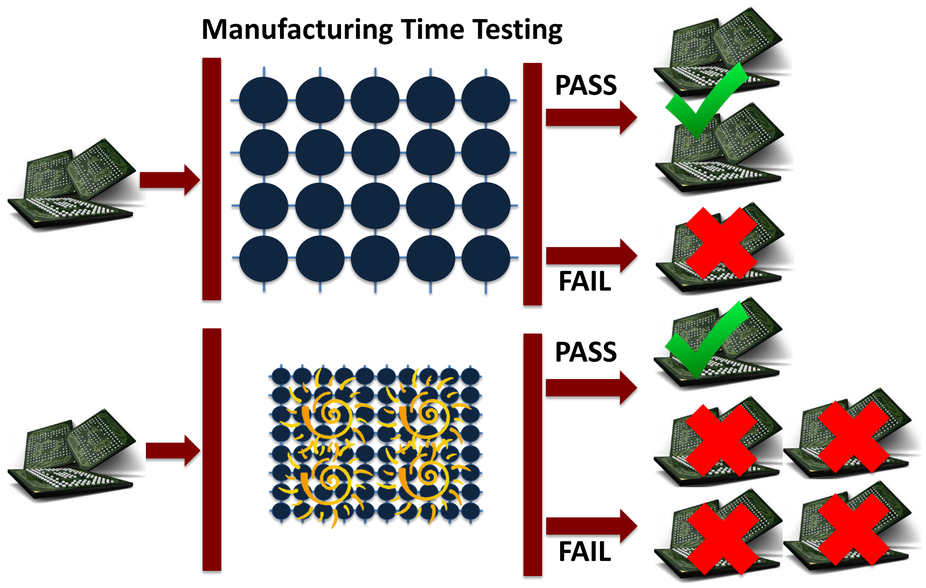
DRAM SCALING PROBLEM

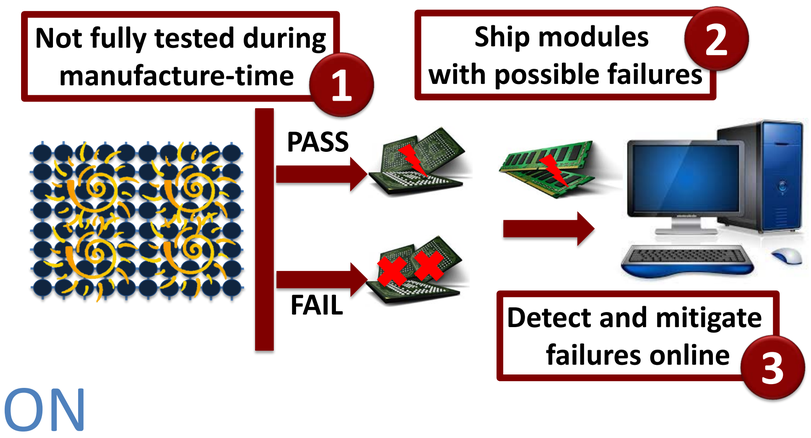


- **Scaling DRAM cells results in more failures**
  - More interference among cells
- Some retention failures are intermittent
  1. **Data Pattern Dependence**
  2. **Variable Retention Time**
- Detecting intermittent failures is hard
- Longer manufacture-time tests
- Lower yield
- Higher cost



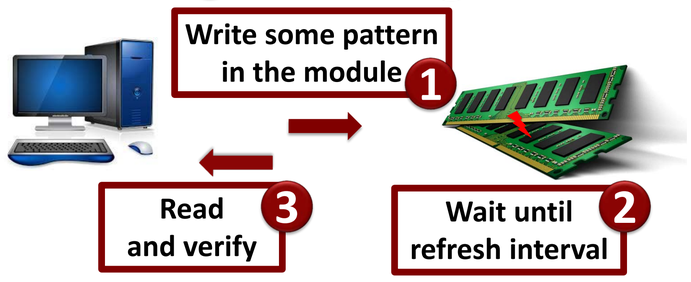
VISION: ONLINE PROFILING

- **Detect and mitigate errors after the system has become operational**
- Reduces cost of testing, increases yield, enables scaling
- **In order to design such a system, we need to know the effectiveness of system-level detection and mitigation techniques**
- **We analyze the efficacy of some simple techniques and recently proposed techniques using experimental data from real DIMMs**

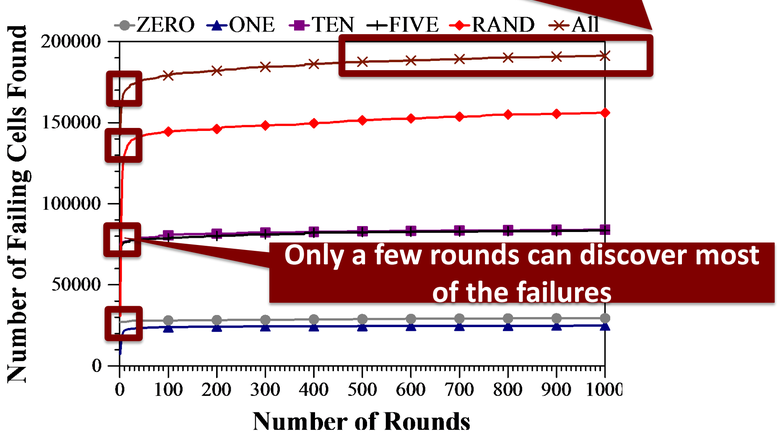


EFFICACY OF SYSTEM-LEVEL DETECTION AND MITIGATION

1 Testing



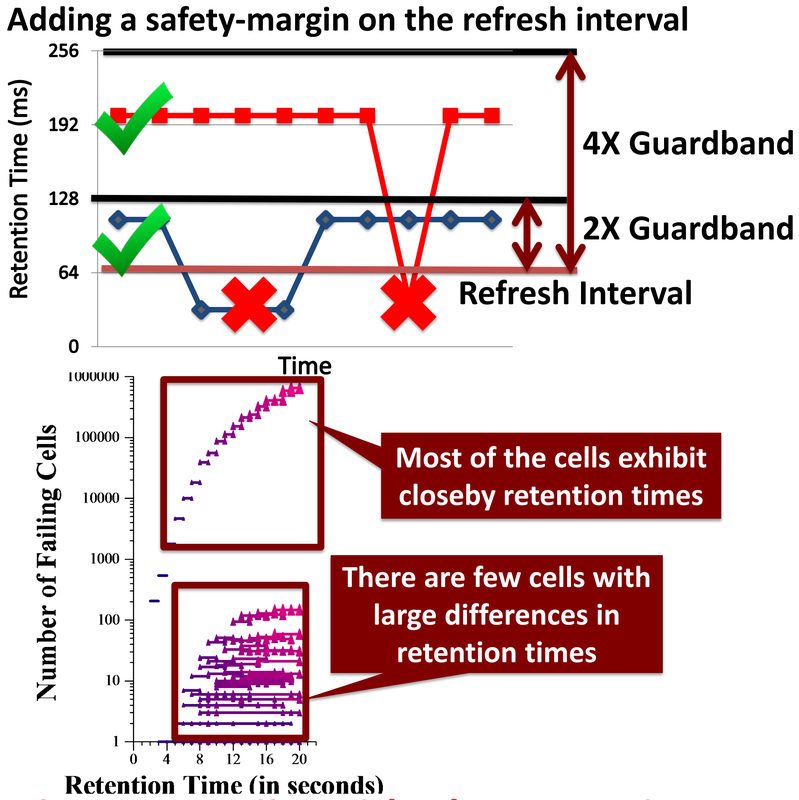
Even after hundreds of rounds, a small number of new cells keep failing



Testing alone cannot detect all possible failures

2 Guardbanding

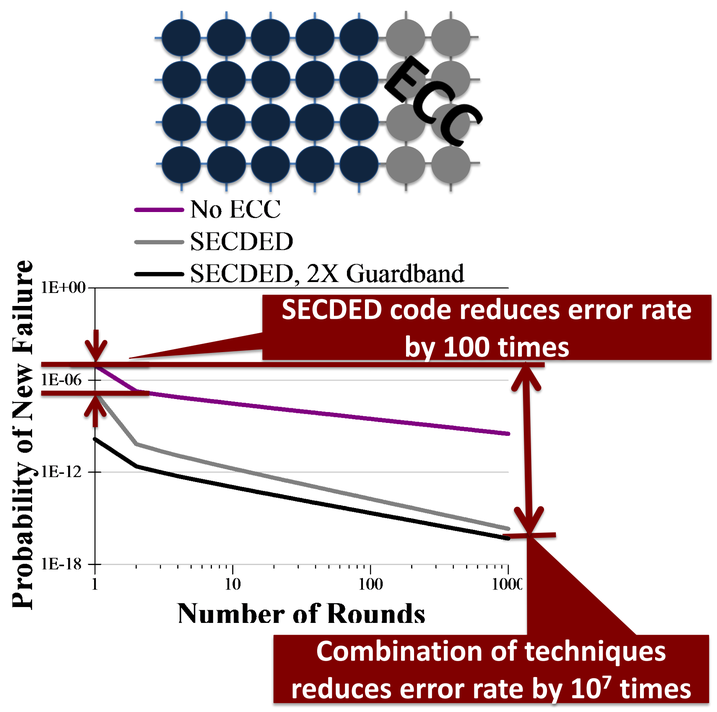
Adding a safety-margin on the refresh interval



Even a large guardband (5X) cannot detect 5-15% of the intermittently failing cells

3 Error Correcting Code

Additional information to detect error and correct data

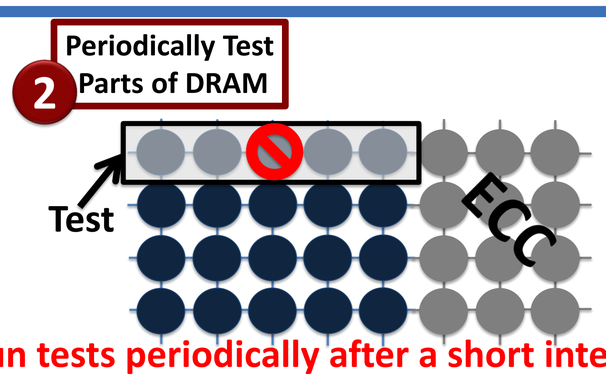


A combination of mitigation techniques is much more effective

TOWARDS AN ONLINE PROFILING SYSTEM

Key Observations so far:

1. Testing alone cannot detect all possible failures
2. Combination of ECC and other mitigation techniques is much more effective
   - But degrades performance
3. Testing can help to reduce the ECC strength
   - Even if we start with a higher strength ECC



Run tests periodically after a short interval at smaller regions of memory

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